IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of
Ham III.

Serial No.: **09/747,052**

Filed: **22 December 2000**

For: **CLOCK SYNCHRONIZATION IN A COMMUNICATIONS ENVIRONMENT**

Attorney's Docket No: **4015-808**

Patent Pending

Examiner: Ted Wang

Group Art Unit: 2611

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REPLY BRIEF

Dear Sir or Madam:

This paper is timely submitted in reply to the Examiner's Answer mailed on 23 February 2007. The following remarks stand in addition to those made of record in Applicant's Appeal Brief, and directly respond to the Examiner's Answer. No fees should be required for entry of this paper, but the Commissioner is hereby authorized to charge any fees that are required to Deposit Account 18-1167.

I. STATUS OF CLAIMS

Claims 1-7, 10-16, 18, 24-26, 32-35, 37, and 39 stand rejected by the examiner. Claims 8, 9, 17, 19-23, 27-31, 36, and 38 are objected to as allowable but for their dependence on a rejected base claim. The rejection of claims 1-7, 10-16, 18, 24-26, 32-35, 37, and 39 is on appeal.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

In the Final Office Action, the examiner rejected claims 1-7, 10, 11, 13-16, 18, 24-26, 32, and 37 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,909,148 to Tanaka (hereinafter "Tanaka"). In the Examiner's Answer to Applicant's Appeal Brief, the examiner withdraws the 102(b) rejection of dependent claims 5-7, 13-16, and 18, but maintains the remaining 102(b) rejections.

Further in the Final Office Action, the examiner rejected claims 34, 35, and 39 under 35 U.S.C § 103(a) as being anticipated by Tanaka in view of U.S. Patent No. 6,353,647 to Wilhelmsson et al. (hereinafter "Wilhelmsson"). The examiner maintains these rejections in the Examiner's Answer.

Finally, in the Final Office Action, the examiner rejected claims 12 and 33 under 35 U.S.C § 103(a) as being anticipated by Tanaka in view of U.S. Patent No. 5,619,543 to Glass et al. (hereinafter "Glass"). The examiner withdraws these rejections in the Examiner's Answer.

III. ARGUMENT

A Fundamental Shortcoming of All Claim Rejections

In the Examiner's Answer, the examiner acknowledges that Tanaka does not teach the use of "averaged control values" for PLL loop filter updating—see pp. 15 and 16 of the Answer. Applicant appreciates that these remarks by the examiner are set in the context of dependent claims offering additional limitations over the corresponding independent claims. However, the

"averaged control values" at issue in these claims relate directly back to the antecedent term appearing in the independent claims at issue.

Thus, when the examiner acknowledges and agrees with Applicant's articulated explanation that Tanaka does not generate averaged control values from filter 11, but rather determines time-change values from filter 11—i.e., step changes between the output of filter 11 at a previous time and at a current time—it appears that all of the examiner's anticipation and obviousness rejections are undone, and not just those rejections made against these particular dependent claims. See, for example, lines 2-4 on p. 16, where the examiner finds persuasive Applicant's prior argument that "'[t]hose change values are filtered by element 15. The change values are not control values as output by filter element 11, and the averaged change values of Tanaka are not averaged control values within the meaning of Applicant's claims.'" (Emphasis added.)

If the examiner acknowledges and finds persuasive the argument that Tanaka does not teach the use of averaged control values—i.e., averaged values obtained by averaging the control values output by a PLL loop filter—within the meaning of Applicant's claims, then by definition all of the rejection arguments should be withdrawn because all arguments rely on the mistaken assertion that Tanaka provides such teachings. This point is explored in more detail below.

The Claimed PLL Output Signal Arguments

The Applicant and examiner have long been arguing over whether the signal output from NCO 9 is a PLL output clock signal within the meaning of the claims rejected as anticipated by Tanaka. In an apparent tacit recognition that NCO 9 does not produce a PLL output clock signal within the meaning of Applicant's claims, the Examiner's Answer now advances a new argument, namely, that the PLL output clock signal at issue in the rejected claims comes from a counter/divider 78 (shown in Fig. 5 of the instant application) rather than from a voltage

controlled oscillator (VCO) 74, and, therefore, that Applicant has confused its own terms and that the signal being argued for by Applicant really is an internal PLL signal, and thus more directly compares with the internal signal from NCO 9 of Tanaka. This new line of argument is without any merit and is contradicted by a plain understanding of PLL circuits, by the explicit language of the instant application, and, most critically, by the plain language of the claims.

Specifically, at the bottom of p. 9 through p. 12 of the Examiner's Answer, the examiner states that Applicant has "confused his own design terms" because the output of the voltage controlled oscillator (VCO) 74 in Fig. 5 of the instant application, which is the VCO controlled by the claimed control values, produces an internal signal rather than the claimed PLL output clock signal as has been argued. Presumably, if VCO 74 produces an internal signal, then the examiner believes his comparison to the output of NCO 9 of Tanaka is valid.

It is not an oversimplification to say that the thrust of the examiner's (anticipation) rejection arguments has been that Numeric Controlled Oscillator (NCO) 9 of Tanaka, such as shown in Fig. 1 of Tanaka, is the same as the PLL output clock signal at issue in all of the claims rejected as anticipated by Tanaka. Applicant has repeatedly pointed out that Tanaka teaches an Automatic Frequency Correction (AFC) circuit whose final output is a DEMODULATED SIGNAL—see Fig. 1 of Tanaka. In that context, Tanaka explicitly states that, "[t]he oscillating frequency of the second NCO 9 is controlled so that it becomes the residual frequency error of the AFC loop." (Tanaka, col. 5, lines 43-45.)

In contrast, the PLL output signal in the rejected claims at issue is an overall PLL output signal, e.g., the output from the PLL module 62 described in the instant application. The distinction is important because the rejected independent claims carefully and explicitly describe deriving control values for controlling the PLL based on filtering successive phase differences between a reference clock signal and the PLL output signal. Further, the rejected independent claims carefully and explicitly claim adapting or adjusting the (loop) filter used to generate the

control values based on averaging the control values. It is key, then, that the control values used to close the PLL frequency control loop—i.e., the overall PLL frequency control loop—are the values averaged to obtain a basis for adapting the PLL loop filter.

Even a cursory inspection of NCO 9 in Tanaka reveals that it does not and can not perform the claimed functions, and cannot serve as a basis for anticipation of the rejected claims. Indeed, the whole thrust of the examiner's argument misses the fundamental point. With reference to Fig. 5 of the instant application, which the examiner refers to in the Examiner's Answer, VCO 74 does produce the claimed PLL output clock signal because its output signal is the one fed back for phase difference comparison and it is the signal whose frequency is controlled by the PLL's closed loop control to take on the desired value relative to the input reference clock signal. Anyone skilled in the art would appreciate that all of those distinctions hold true regardless of whether the output clock signal from the VCO 74 is fed back to the phase comparator 66 through a simple counter/divider 76, and regardless of whether the output clock signal 74 is passed through a simple counter/divider 78 at the output of the PLL module 62.

It is erroneous, then, for the Examiner's Answer at p. 11 to state that the output of Applicant's VCO 74 is an internal signal to Applicant's PLL module 62. See lines 16-17 on p. 9 of the instant application as filed, wherein applicant explains that, "[t]he oscillator 74 generates the output clock at a frequency determined by the oscillator control signal." That definitively identifies VCO 74 as producing the output signal of the PLL module 62. See, also, lines 24-26 on p. 11 of the instant application, wherein Applicant explains that, "...the oscillator 74 might be a voltage-controlled oscillator (VCO) generating an output signal at a clock frequency responsive to the control signal." Also, at p. 11, line 26 – p. 12. line 2, the application explains that, "...the loop filter 68 generates digital control values that set the output voltage of a DAC

(i.e., the oscillator controller 72), which in turn controls the oscillation frequency of the VCO 74." (Emphasis added.)

In contrast, from Fig. 1 of Tanaka, one sees that NCO 9 generates a residual frequency error signal, which operates as a control input for a complex multiplying device 8 that performs a frequency conversion on the signal output by Tanaka's low pass filter 6. (See Tanaka at col. 3, line 61 and Abstract.) It is beyond argument that the "output signal" from NCO 9 is an internal, residual frequency error (for AFC correction) of the AFC circuit of Tanaka, and cannot be equated with the claimed PLL output clock signal of the rejected claims. For this reason alone, the rejection arguments based on Tanaka fail as a matter of law.

The Filtering Adaptation Arguments

As an example of the filtering claim limitations rejected as anticipated by Tanaka, claim 1 claims "adapting a filter used to filter said successive phase difference values based on average control values determined from said successive control values." As elsewhere, it is key to recognize that the claimed phase difference values are derived from the overall PLL output signal and an input reference signal, and are filtered to obtain control values for controlling the overall PLL output signal. Thus, the examiner is not free to find any filtering function in Tanaka and then argue *anticipation* of the claim limitation.

On p. 13 of the Examiner's Answer, the examiner states that:

> From the teachings of Tanaka's reference it is clear that the PLL (Fig. 1, elements 8-11, 13-16, 101 and 102) circuit adapts a (PLL) loop filter 11 based on averaging (Fig. 1 element 15) the PLL frequency control values output (Fig. 1 element g(nT)) by that loop filter.

The above argument is off point. Fig. 1 of Tanaka does show a loop filter 11, but it is controlled (adapted) by a PLL controller 102, which takes its control values from a memory 101, which Tanaka (col. 4, lines 3-7) explains as containing loop control parameters that are accessed by

the PLL controller to set the loop filter 11. See, also, lines 18-23 of col. 4 in Tanaka for an explicit explanation of the controller 102 using stored values in memory 101 to adapt filter 11.

The examiner seems to be confusing the averaging property of filter 11 with the claimed step of adapting a PLL loop filter based on the average of the control values output by that filter. In other words, Tanaka's filter 11 may produce "averaged" values, indeed, that is a common filter function, but that function has nothing to do with taking the filter's output, averaging those values, and then adapting the filter's response based on the average of the filter's output. In this fundamental aspect of the rejection, the examiner's anticipation arguments are directly contradicted by Tanaka. For this reason alone, the rejection arguments based on Tanaka fail as a matter of law.

Further, the examiner alleges that the instant specification does not disclose the claimed filter adaptation, see p. 12 of the Examiner's Answer. Applicant disagrees. For example, the last line on p. 2 of the instant application states that, "[f]ilter settings and state transitions are based on processing averaged control output values." See, also, p. 3, lines 16-24, which explicitly describes Proportional-Integral (PI) filter coefficient updating as a function of the average of the digital-analog-converter (DAC) control values being generated from reference-to-output clock signal phase differences. See, also, p. 16, lines 6-16, for a detailed presentation of control value averaging. In short, the claimed operation of updating the PLL loop filter used to generate PLL control values as a function of averaged control values is well supported in the application as filed.

Dependent Claims 2-4 Arguments

Beginning at the last line on p. 14 of the Examiner's Answer, the examiner acknowledges that Tanaka does not teach updating filter 11 based on averaging its output values. That admission wholly undercuts the legal foundation of the anticipation rejection against these claims. To counter that problem, the examiner states that the PLL controller 102

updates the filter 11 based on a determined signal from data determining unit 16, which in turn is based on the average of g(nT) values output by the filter 11. However, these arguments are flatly contradicted at p. 16 of the Examiner's Answer, where the examiner acknowledges that Tanaka does not teach "averaged control values" within the meaning of Applicant's claims in the context of claims 5-7, 13-16, and 18.

In more detail, in continuing the rejection of claims 2-4, the examiner refers to col. 5, line 42 – col. 6, line 6 of Tanaka for support of that assertion, but that section of Tanaka directly contradicts the examiner. First, the average of g(nT) is never determined in Tanaka. Instead, the data determining unit 16 "wants" to know what the time-change (delta) is for g(nT) over a defined time interval. To that end, a subtracting device subtracts a previous value of g(nT), as provided by delay unit 13, from a current value of g(nT), and the data determining unit compares that time-change value to a threshold. Thus, the determined signal is not an average of the output from filter 11, nor is it based on the average of output values from filter 11.

At most, one can say the determined signal from unit 16 is based on the average of time-change values, which are obtained by subtracting old g(nT) values from new g(nT) values. Further, the examiner's arguments miss the overarching point that the output values from filter 11 are not overall PLL control values for controlling the PLL output clock signal as Applicant claims, but rather values associated with a residual frequency error of the AFC function of Tanaka.

Note, too, that claims 2-4 explicitly claim taking filter adaptation steps as a function of detecting a trend in the averaged control values—i.e., the average of the control values output by a PLL loop filter. The examiner states that the data determining unit 16 of Tanaka responds to trends by detecting whether the output from averaging circuit 15 is "large towards a threshold." That statement is inaccurate. Averaging circuit 15 of Tanaka operates on delta values (time-change values) formed by subtracting old g(nT) values previously output by filter

11 from new g(nT) values. These time change values are the control values themselves and the averaging circuit 15 therefore does not produce averaged control values. Moreover, the data determining unit 16 does not detect trends in the output of averaging circuit 15, it merely performs a threshold comparison—the values output by the averaging circuit 15 could trend up and down to any extent less than the threshold used by unit 16, and no filter adaptation would take place, because none of that trending would trigger the threshold comparison function of unit 16.

Dependent Claims 34, 35, and 39

Beginning on p. 17 of the Examiner's Answer, the examiner defends the obviousness rejection of claims 34, 35, and 39 based on the argued-for combination of Tanaka and Wilhelmsson, by reinforcing arguments about the equivalency between analog control of a VCO via analog outputs from a DAC and digital control of an NCO. All of these rejected dependent claims depend from claim 24, which explicitly directs itself to a PLL that provides an output signal in a manner consistent with the other dependent claims and not taught by Tanaka.

Therefore, it misses the point to argue that one might be motivated to substitute Wilhelmsson's DAC/VCO for Tanaka's NCO, because neither Tanaka nor Wilhelmsson, taken in any combination, teach or suggest the limitations of the independent claim from which these claims depend. Moreover, the examiner's original motivation arguments rested on the assertion that one skilled in the art would have been motivated to make the substitution of Wilhelmsson's teachings into Tanaka to reduce circuit board size and reduce circuit cost. It is unclear how the Examiner's Answer at line 11 of p. 18 squares with that assertion—i.e., how does substituting a DAC plus a VCO (two elements involving digital-to-analog domain transformation) for one NCO (a digital domain device) yield size reductions and/or cost savings?

Still further, Tanaka teaches that a PLL controller 102 interfaces with a digital memory circuit 101 to read out parameter values for use in setting the NCO 9. These operations all

clearly take place within the digital domain of Tanaka, and it is illogical for the examiner to argue that one would be motivated to substitute two components from Wilhelmsson, including one that made an unneeded and undesired digital-to-analog domain transformation, for Tanaka's one NCO 9. Indeed, the real motivation to use Wilhelmsson seems to come from the examiner's desire to find a reference that disclosed a DAC/VCO arrangement irrespective of whether that arrangement combined in any sensible way with Tanaka.

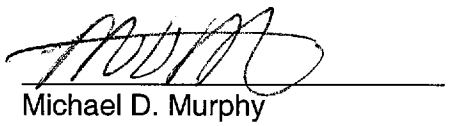
Finally, with respect to the specific arguments provided at p. 19 of the Examiner's Answer in support of the rejection of claim 39, it is enough simply to reiterate that Tanaka and Wilhelmsson, taken alone or in any combination, do not teach or suggest the limitations of the independent claim (24) from which claim 39 depends. Therefore, the examiner's attempt to equate a combination of processing elements from Tanaka with the claimed digital processor of claim 39 is without merit because the combination of elements grouped together by the examiner does not perform the functions attributed to the claimed digital processor.

Closing

In view of the above remarks and the remarks of the previously filed Appeal Brief, Applicant submits that all claim rejections fail as a matter of law, and that the pending claims stand in condition for allowance over the cited references. Applicant therefore respectfully requests that the Board overturn the examiner's rejections.

Respectfully submitted,

COATS & BENNETT, P.L.L.C.



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